IN THE CLAIMS

Claims 23-25 and 29-31 are canceled without prejudice.

1. (Previously Presented) A method of patterning a crystalline film comprising:

forming a crystalline film having a degenerate lattice comprising first atoms in a first region and a second region;

placing dopants into interstitial cites in said crystalline film in said first region wherein said dopants are electrically neutral with respect to said crystalline film;

activating said dopants so that said dopants substitute with said first atoms in said lattice to form a non-degenerate lattice in said first region, said second region remaining a degenerate lattice; and

exposing said first region and said second region to a wet etchant wherein said wet etchant etches said degenerate lattice in said second region without etching said non-degenerate lattice in said first region.

2. (Original) The method of claim 1 wherein said crystalline film is a semiconductor film.

3. (Original) The method of claim 2 wherein said semiconductor film is a silicon film.

4. (Original) The method of claim 3 wherein said silicon film is a polycrystalline film.

5. (Original) The method of claim 1 wherein said crystalline film is selected from the group consisting of gallium arsenide and InSb.

6. (Original) The method of claim 1 wherein said etchant utilizing an associative reaction to etch said degenerate lattice.

7. (Original) The method of claim 3 wherein said etchant is a non-oxidizing basic solution.

8. (Original) The method of claim 7 wherein said etchant comprises a hydroxide with a pH between 9 and 11.

9. (Original) The method of claim 5 wherein said etchant comprises an oxidant in the presence of an acid.

10. (Original) The method of claim 9 wherein said etchant comprises an oxidant selected from the group consisting of nitric acid and hydrogen peroxide and wherein said etchant has a pH between 2 and 4.

11. (Original) The method of claim 1 wherein said non-degenerate lattice in said first region has a first lattice energy and said degenerate lattice in said second region has a second lattice energy wherein said second lattice energy is thermodynamically higher (relatively less stable) than said first lattice energy.

12. (Original) The method of claim 1 wherein said non-degenerate lattice has a first activation energy barrier to said etchant and said degenerate lattice has a second

activation energy barrier to said etchant wherein said second activation energy barrier is less than said first activation barrier.

13. (Original) The method of claim 12 wherein said etchant has a chemical energy greater than said second activation energy barrier and less than said first activation energy barrier.

14. (Previously Presented) A method of patterning a crystalline film comprising:

forming a mask having an opening on a crystalline film having a lattice comprising first atoms, said opening formed over a first region and said mask covering a second region;

implanting dopants atoms through said opening and into said first region of said crystalline film beneath said opening wherein said dopant atoms are physically larger than said first atoms;

removing said mask;

heating said crystalline film so that said dopants substitute with said first atoms in said lattice in said crystalline film in said first region; and

exposing said first region and said second region to an etchant wherein said etchant etches said second region without etching said first region.

15. (Original) The method of claim 14 wherein the lattice comprising dopants in said first region is a non-degenerate lattice.

16. (Original) The method of claim 15 wherein said lattice in said second region is a degenerate lattice.

17-19. (Canceled)

20. (Previously Presented) A method of patterning a crystalline film comprising:

providing a crystalline film having a degenerate lattice comprising first atoms in a first region and a second region;

substituting dopant atoms with said first atoms in said degenerate lattice in said first region to form a non-degenerate lattice in said first region wherein said dopants are electrically neutral with respect to said crystalline film; and

exposing said first region having said non-degenerate lattice and said second region having said degenerate lattice to an etchant wherein said etchant etches said second region and not said first region.

21. (Original) The method of claim 20 wherein said crystalline film is silicon.

22. (Currently Amended) The method of claim [[21]] 20 wherein said dopant atoms are boron.

23.- 25. (Canceled)

26. (Original) A method of forming integrated circuit comprising:

forming a sacrificial gate electrode over a first channel region of a semiconductor substrate and forming a second sacrificial gate electrode over a second channel region of said semiconductor substrate;

altering said first sacrificial gate electrode and/or said second sacrificial gate electrode such that said first sacrificial gate electrode can be etched with an etchant without etching said second sacrificial gate electrode;

forming a dielectric layer over said first sacrificial gate electrode and over said second sacrificial gate electrode;

planarizing said dielectric layer so as to exposed the top surface of said first sacrificial gate electrode and said second sacrificial gate electrode;

after altering said first sacrificial gate electrode and/or said second sacrificial gate electrode etching said first sacrificial gate electrode with said etchant without etching said second sacrificial gate electrode to form a first opening and expose said first channel region of said semiconductor substrate;

depositing a first metal film over said first channel region of said semiconductor substrate and on the top surface of said dielectric film;

removing said first metal film from the top of said dielectric to form a first metal gate electrode;

removing said second sacrificial gate electrode material to form a second opening;

forming a second metal film different than said first metal film over said dielectric layer and into said second opening; and

removing said second metal film from the top surface of said dielectric layer to form a second metal gate electrode.

27. (Original) The semiconductor device of claim 26 wherein said first metal film has a work function between 3.9 eV and 4.2 eV.

28. (Original) The method of claim 26 wherein said second metal film has a work function between 4.9 eV to 5.2 eV.

29. –31. (Canceled)